**Swagat Panda**

**2017B5A30983P**

**Analog Electronics Lab 1 – CE Amplifier**

**Objectives**

**Design the provided circuit on LT Spice and calculate the following parameters with and without the emitter capacitor:**

A. Voltage gain

B. Input Resistance

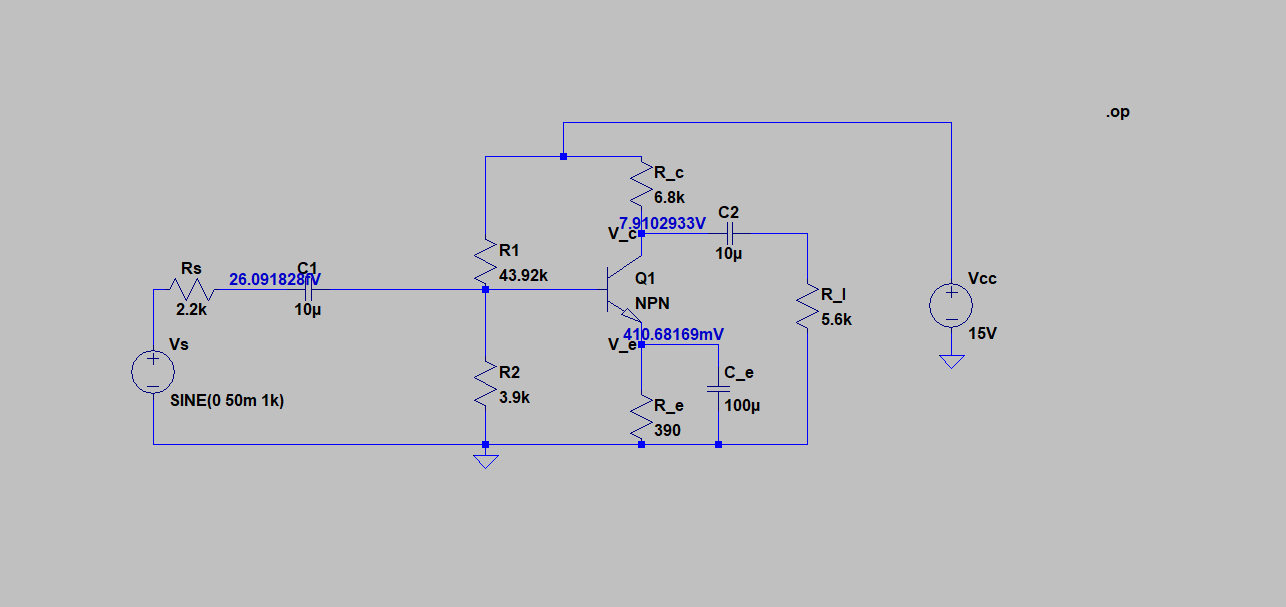
C. Output Resistance

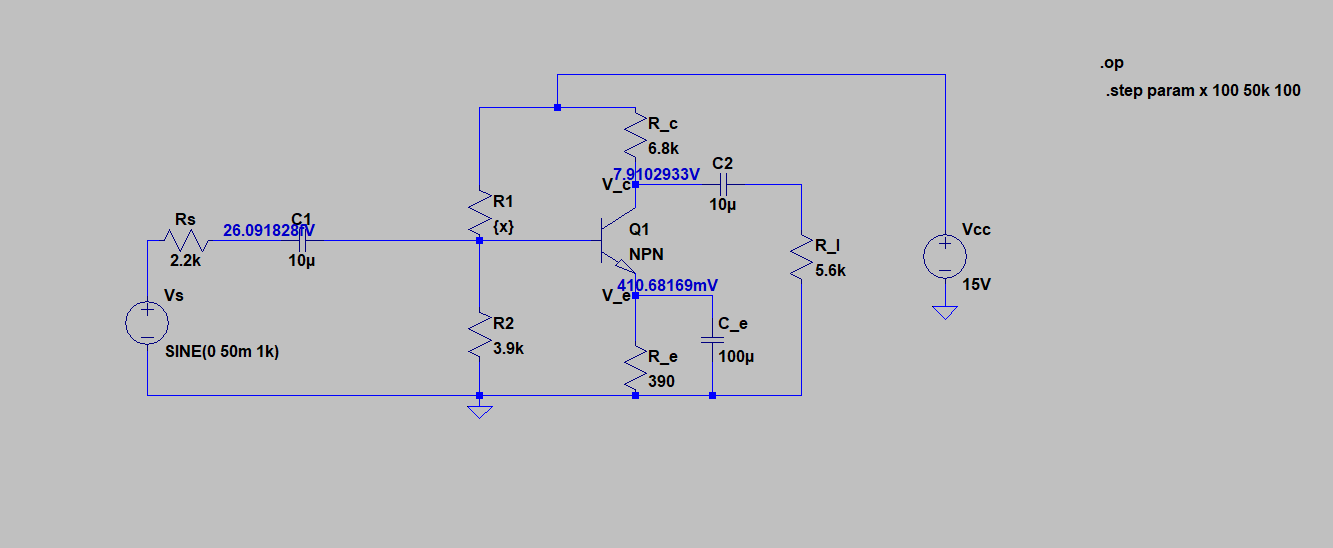
D. Show input and output waveform

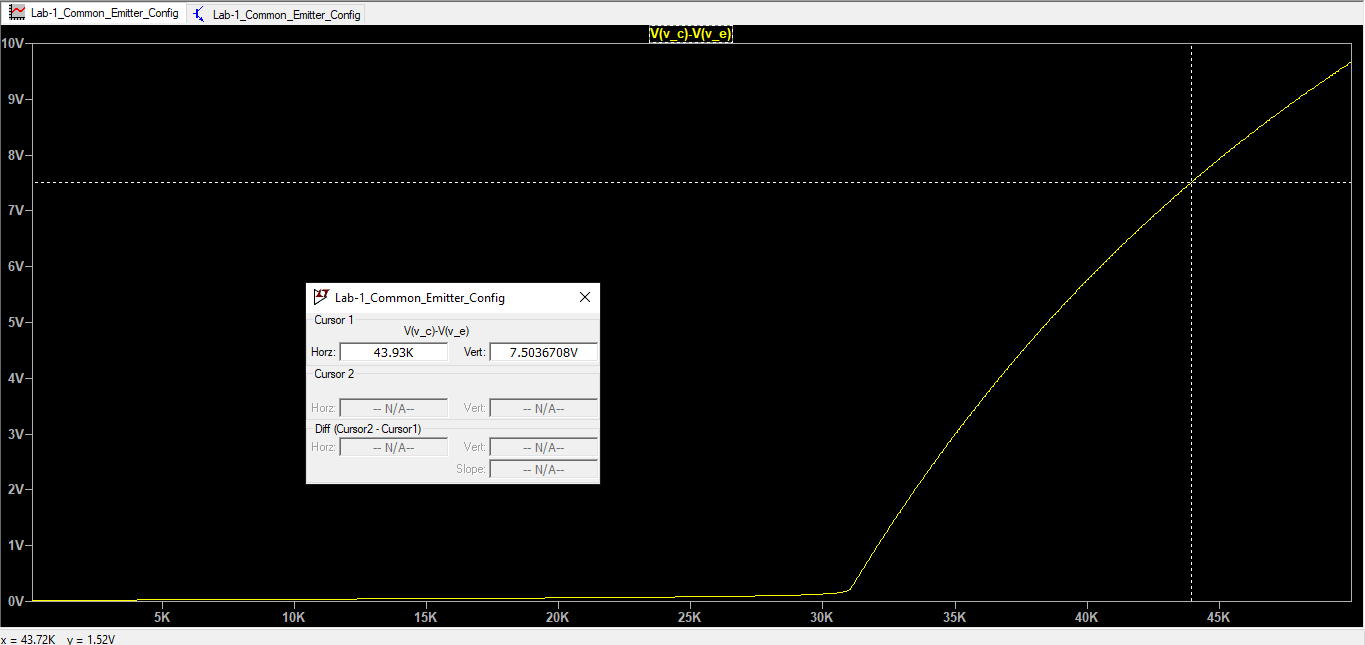
**Components**

* DC Voltage source 15 V
* Resistances of values 6.8 kΩ, 390 Ω, 2.2 kΩ, 3.9 kΩ and 5.6 kΩ
* One variable Resistance
* Capacitors of values 10 μF, 10 μF and 100 μF
* AC voltage source (50mV, 1kHz)

**Determination of the Variable Resistance for the desired Q point**



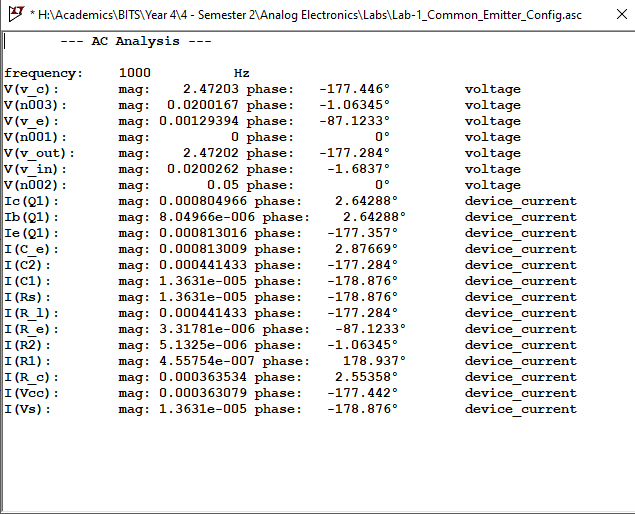




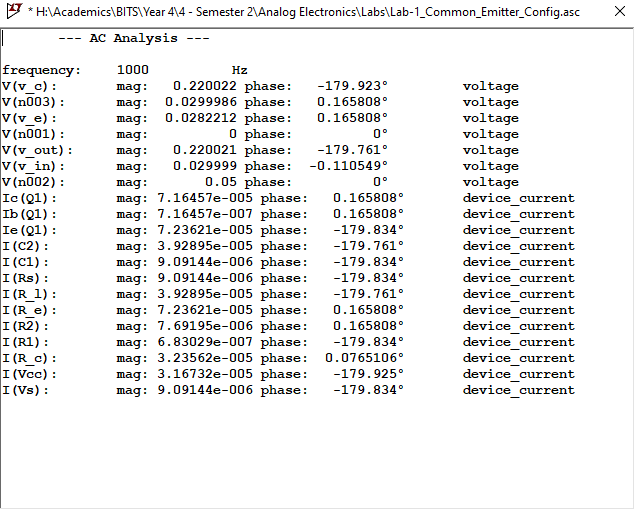
DC Analysis using .op – comes out to be 43.92 k, for .

**.ac Analysis to find the gain at 1 kHz**

Gain with : – 123.43392



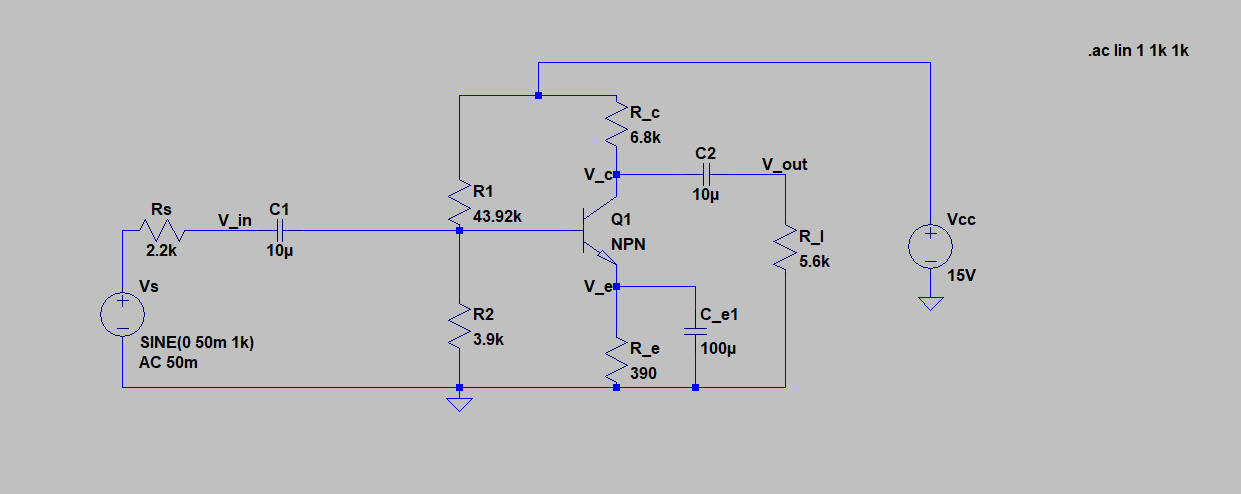
Gain without : – 7.334278

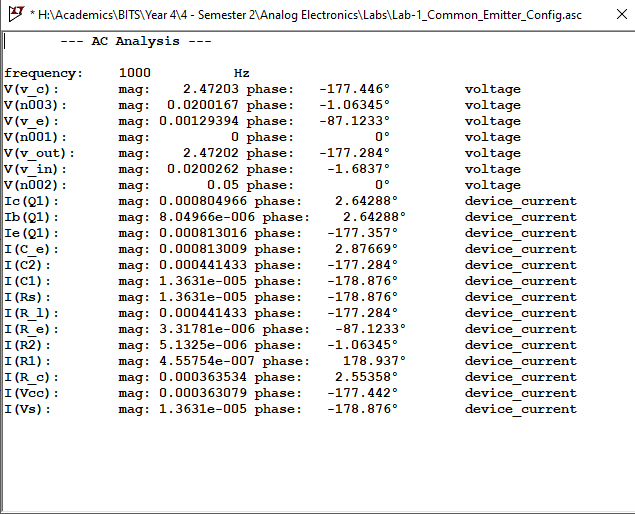


**Input Resistance - with**

DC Input Resistance – Infinity

AC Input Resistance:

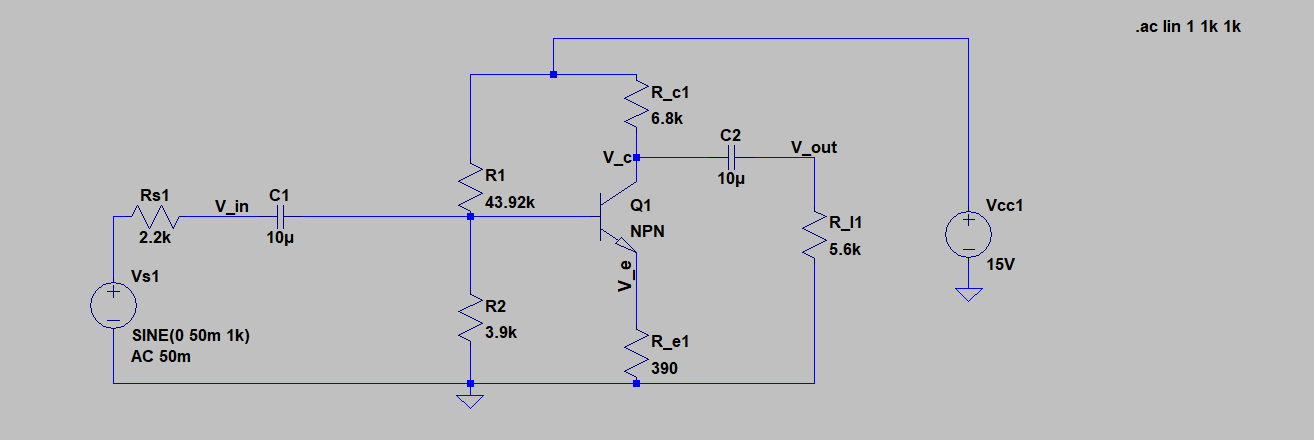


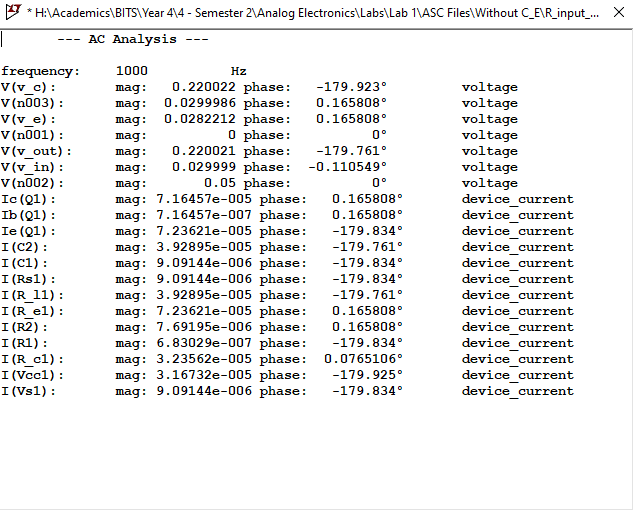


**Input Resistance - without**

DC Input Resistance – Infinity

AC Input Resistance:

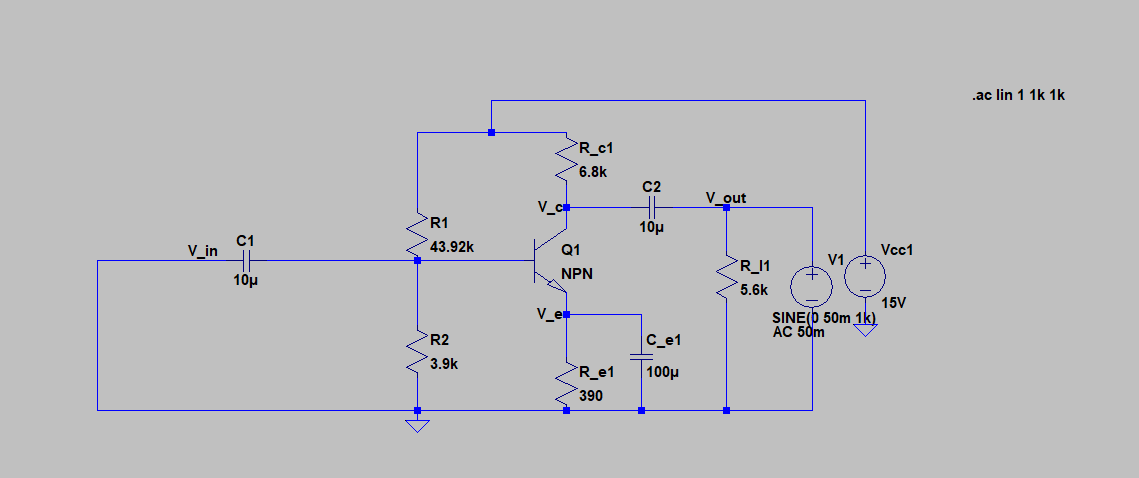


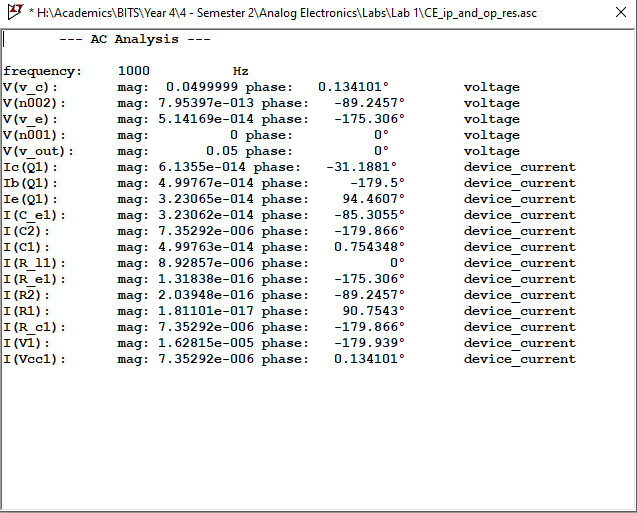


**Output Resistance - of the complete circuit (including ) with**

DC Output Resistance – 5.6

AC Output Resistance:

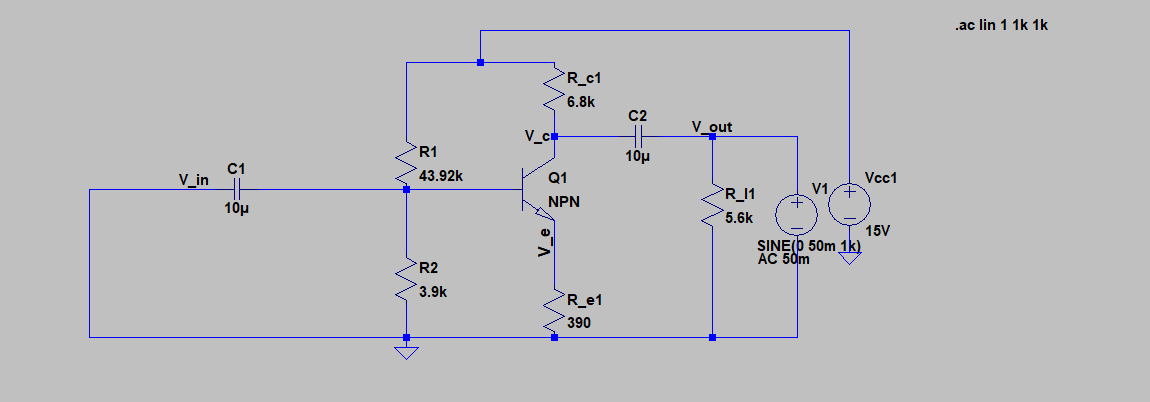


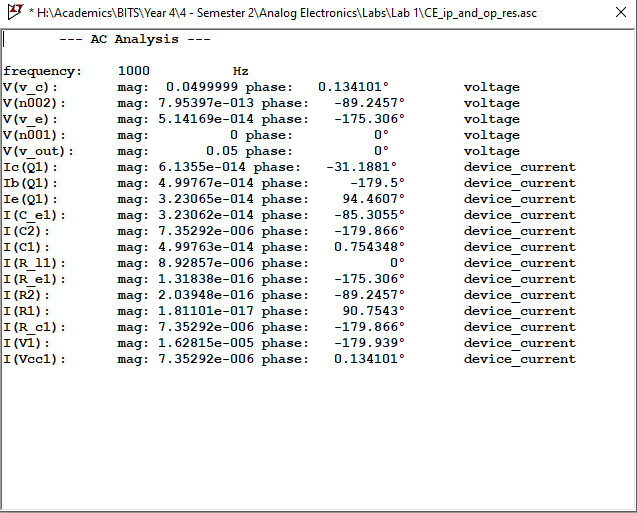


**Output Resistance - of the complete circuit (including ) without**

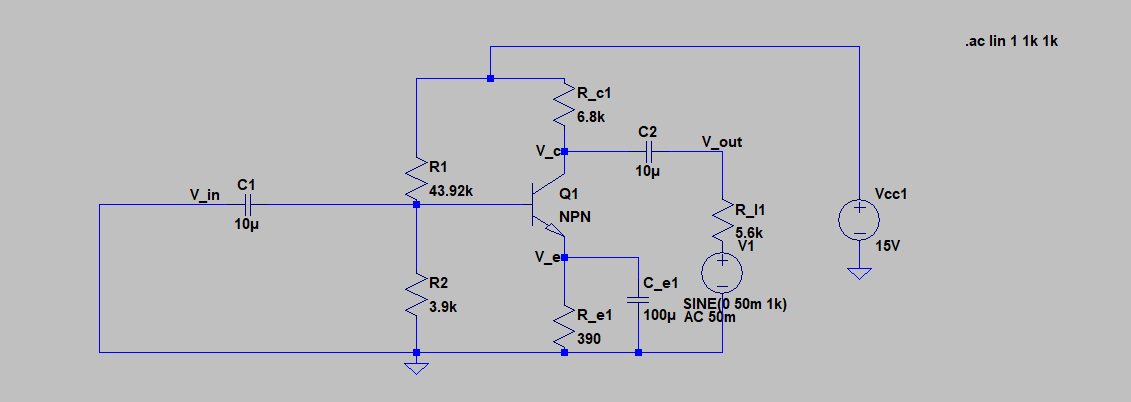
DC Output Resistance – 5.6

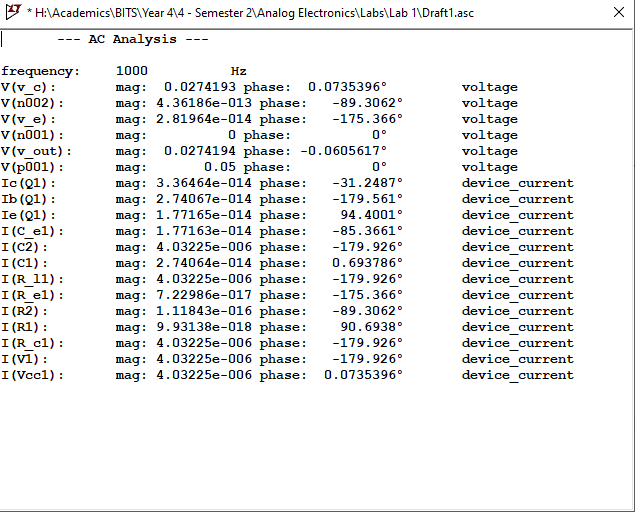
AC Output Resistance:



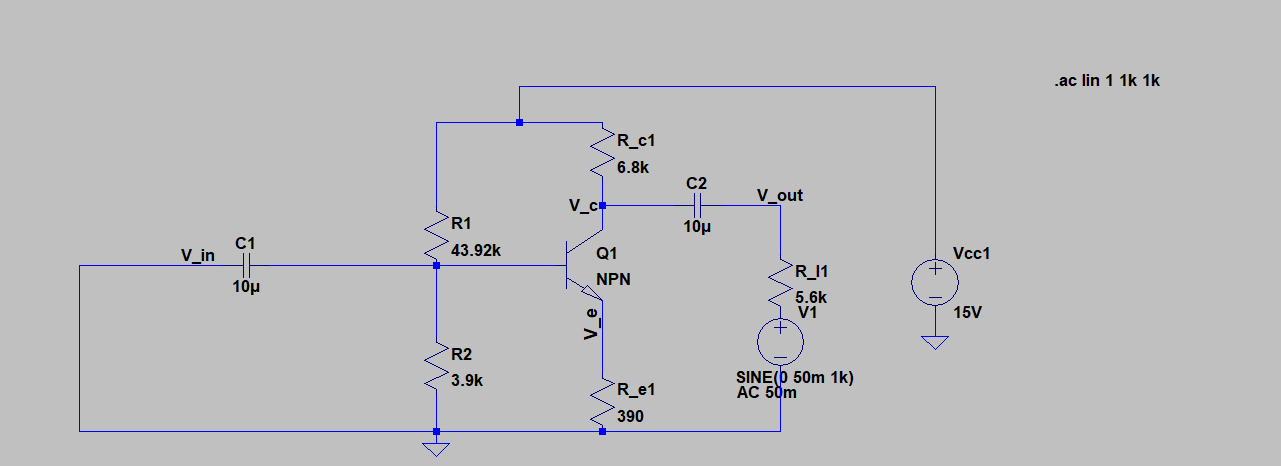


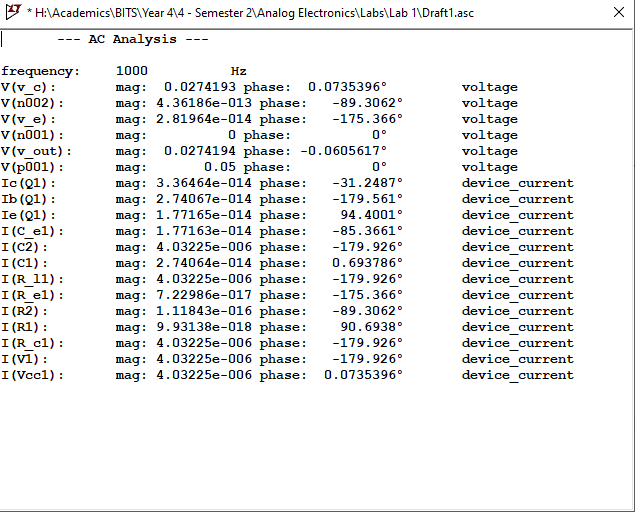
**Output Resistance - of the CE stage only (before ) with**





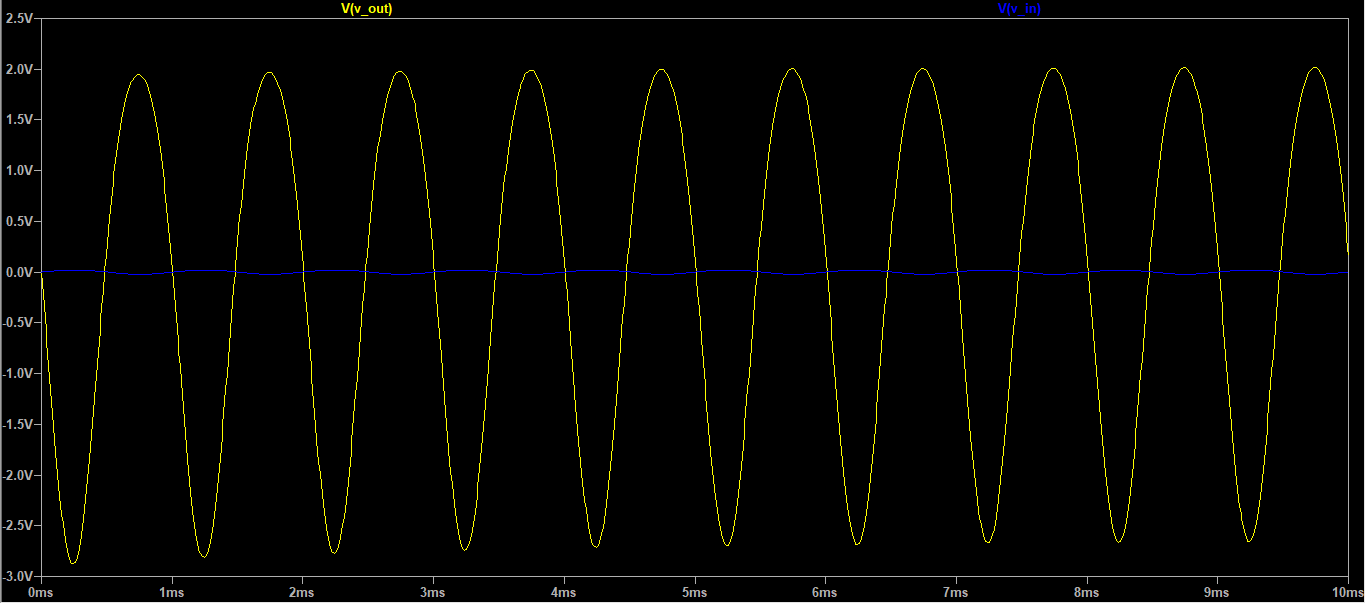
**Output Resistance - of the CE stage only (before ) without**



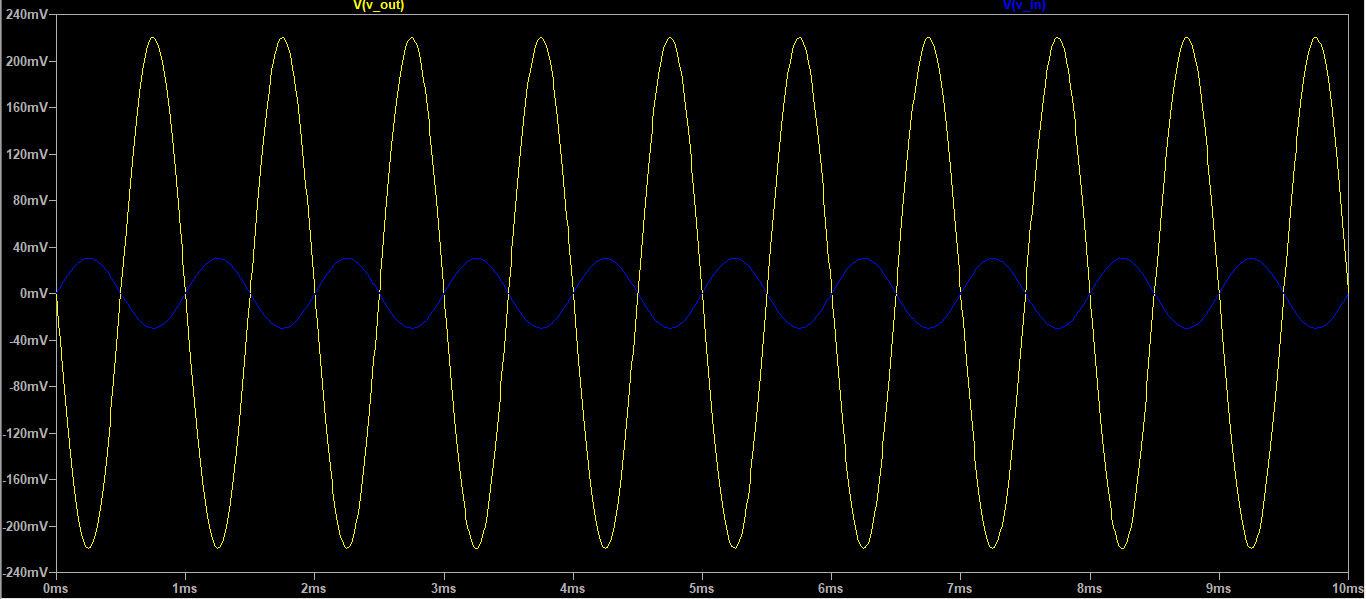


**Input and Output Waveforms**

With



Without



**SPICE Netlist**

Vs N002 0 SINE(0 50m 1k)

R2 Vb 0 3.9k

Re Ve 0 390

C2 Vb Vin 10µ

Rs Vin N002 2.2k

Q1 Vc Vb Ve 0 NPN

R1 N001 Vb 43.92k

Rc N001 Vc 6.8k

Cc1 Vout Vc 10µ

Vcc N001 0 15V

Rl Vout 0 5.6k

C1 Ve 0 100µ

.model NPN NPN

.model PNP PNP

.lib C:\Users\swaga\OneDrive\Documents\LTspiceXVII\lib\cmp\standard.bjt

\*.step param 40k 55k 0.1k

\*.op

\*.ac dec 1 1k 1k

\*.tran 10m

.backanno

.end

**Observations & Conclusions:**

* Common emitter circuit uses “Voltage Divider Biasing”, hence bias at V supply /2, at the Q-point. It gives the best stability.
* BJT in CE configuration, behaves as an inverting amplifier.